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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,519	12/03/2003	Takafumi Yamaji	04329.3190	5009

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EXAMINER	
CHAN, RICHARD	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,519	YAMAJI, TAKAFUMI	
	Examiner	Art Unit	
	Richard Chan	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-10 and 13-17* is/are allowed.

6)☐ Claim(s) *1,2 and 11* is/are rejected.

7)☐ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/3/03 & 11/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoshioka (US 2002/0158789 A1).

With respect to claim 1, Yoshioka discloses the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **Fig.2 circuit 3** including a plurality of **sample-and-hold units 3** which are connected in parallel and selectively activated corresponding to a required resolution to sample and hold an analog input signal from **amplifiers 2**; a plurality of **conversion stages 5** connected in cascade to an output of the **sample-and-hold circuit 3** to convert an output signal of the sample-and-hold circuit to a plurality of bit signals; and a **synthesis circuit 6** to synthesize the bit signals to generate a digital output signal. Paragraphs [0057-0059]

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka (US 2002/0158789 A1) in view of Velazquez (US 5,568,142).

With respect to claim 2, Yoshioka discloses the variable resolution analog-to-digital converter according to claim 1, Yoshioka continues to disclose wherein the conversion stages comprise a plurality of variable conversion stages **5** in cascade to the output of the sample-and-hold circuit **3** and a plurality of non-variable conversion stages in cascade to a last one of the variable conversion stages **5**, each of the variable conversion stages including a first sub-analog-to-digital converter unit configured to convert a first analog signal to a first digital signal **[Paragraph 0057]** however, Yoshioka does not disclose a plurality of first sub-multiplying-digital-to-analog converter units connected in parallel and selectively used according to the required resolution to convert the first digital signal to a second analog signal, generate a first difference signal between the first analog signal and the second analog signal and multiply the first difference signal by a give value, the first analog signal being an analog signal corresponding to the analog input signal.

The Velazquez reference (US 5,568,142) however discloses in Fig.6 digital-to-analog converter units **62** connected in parallel and selectively used according to the required resolution to convert the first digital signal **u(n)** to a second analog signal **xk(t)**, generate a first difference signal between the first analog signal and the second analog signal and multiply with combiner **64** the first difference signal by a give value, the first analog signal being an analog signal corresponding to the analog input signal. **(Col.11 lines 10-31)**

It would have been obvious to one of ordinary skill in the art to implement digital to analog converter as disclosed by Velazquez with the Analog to digital converter circuit as disclosed by Yoshioka in order to reconvert the digital signal from baseband back to an analog signal.

With respect to claim 11, Yoshioka discloses the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **Fig.2 circuit 3**including a plurality of sample-and-hold units **circuit 3** which are connected in parallel and selectively used corresponding to a required resolution to sample and hold an analog input signal; a plurality of conversion stages **conversion stages 5** connected in cascade to an output of the sample-and-hold circuit **3**, each of the conversion stages including a sub-analog-to-digital converter unit **4** configured to convert a first analog signal into a digital signal and a switch **7** which turns on or off according to the required resolution to bypass at least an initial stage of the conversion stages; and a synthesis circuit **6** configured to synthesize digital signals each provided by each of the

conversion stages, to generate a digital output signal, however Yoshioka does not specifically disclose a sub-digital-to-analog converter unit to convert the digital signal into a second analog signal and output a difference signal between the first analog signal and the second analog signal, the first analog signal being an analog signal corresponding to the analog input signal.

The Velazquez reference (US 5,568,142) however discloses in Fig.6 digital-to-analog converter units **62** to convert the digital signal into a second analog signal and output a difference signal between the first analog signal and the second analog signal, the first analog signal being an analog signal corresponding to the analog input signal; **(Col.11 lines 10-31)**

Allowable Subject Matter

5. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 3, Yoshioka disclose the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **Fig.2 circuit 3** including a plurality of sample-and-hold units **3** connected in parallel and selectively activated corresponding to a required resolution to sample and hold an analog input signal; a plurality of first conversion stages **5** connected in cascade to an output of the sample-and-hold circuit, each of the first conversion stages **5** including a first sub-analog-to-digital converter unit **4** configured to convert a first analog signal to a first digital signal and a plurality of first sub-multiplying-digital-to-analog converter units connected in

parallel and selectively activated according to the required resolution to convert the first digital signal to a second analog signal, the Velazquez reference than discloses the process of generate a first difference signal between the first analog signal and the second analog signal and multiply the first difference signal by a given value, the first analog signal being an analog signal corresponding to the analog input signal; however the prior art does not disclose a plurality of second conversion stages connected in cascade to an output of a last one of the first conversion stages, each of the second conversion stages including a second sub-analog-to-digital converter unit configured to convert a third analog signal into a second digital signal and a second sub-digital-to-analog converter unit to convert the second digital signal into a fourth analog signal and output a second difference signal between the third analog signal and the fourth analog signal, the third analog signal being an analog signal corresponding to the analog input signal; and a synthesis circuit to synthesize the first digital signal output from each of the first conversion stages and the second digital signal output from each of the second conversion stages, to generate a digital output signal.

Claims 4-10, and 17 are dependent on allowable claim 3.

With respect to claim 12, Yoshioka and Velazquz combined disclose the variable resolution analog-to-digital converter according to claim 11,however the prior art does not disclose the converter further includes a clock phase inverting circuit configured to inverse, when the switch turns on, a phase of a clock signal supplied to the conversion

stages except for at least the initial one of the conversion stages with respect to a phase of the clock signal when the switch turns off.

With respect to claim 13, Yoshioka discloses the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **3** including a plurality of sample-and-hold units **3** which are connected in parallel and selectively used according to a required resolution to sample and hold an analog input signal; a plurality of unit delay circuits **1806** connected in cascade to delay an output signal from the sample-and-hold circuit; **(Paragraph 0021]** an analog linear transformation circuit to subject a set of output signals from the unit delay circuits to a first linear transformation to output a plurality of linear transformed analog signal; a plurality of sub-analog-to-digital converter units **4** to convert the linear transformed analog signal into a plurality of digital signals; however the prior art does not disclose wherein a digital linear transformation circuit to subject a set of digital signals of the digital signals output from the sub-analog-to-digital converter units to a second linear conversion that is an inverting transformation of the first linear transform, to output a plurality of digital signals output by the sub-analog-to-digitals; and a digital delay adder circuit to add the linear digital signals with the same delay time as that of the analog delay circuit to generate a digital output signal.

Claims 14-16 are dependent on allowable claim 13.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Mangelsdorf reference (US 4,924,227) discloses a parallel analog to digital converter.

The Malo reference (US 4,937,579) discloses a method of converting analog signals into digital signals and system for carrying out the method.

The Naylor reference (US 4,940,981) discloses a dual analog to digital converter with single successive approximation register.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chan whose telephone number is (571) 272-0570. The examiner can normally be reached on Mon - Fri (9AM - 5PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571)272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

9/08/06

QUOCHIEN B. VUONG
PRIMARY EXAMINER

Richard Chan
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09/12/06